W. Claim:

1. A process for transmission of a message in a system, said process comprising the steps of sending, receiving, or propagating 1) more than one packet and 2) an Interpacket gap, said packet comprising a start-of-stream delimiter, and a series of at least 16 message bytes encoded in symbols uninterrupted by a control symbol, and said Interpacket gap comprising a plurality of symbols decoded as Idle symbols wherein said Interpacket gap includes at least one non-Idle symbol such that the presence of said non-Idle symbol is part of a message.

2. The process of claim 1 wherein said system comprises Fast Ethernet.

3. The process of claim 2 wherein said non-Idle symbol in said interpacket gap is the symbol for zero.

4. The process of claim 2 wherein said non-Idle symbol is a symbol having only one zero bit.

5. The process of claim 1 wherein said system comprises Gigabit Ethernet.

6. The process of claim 5 wherein said non-Idle symbol comprises a K28.5/Dxx.y or K28.1/Dxx.y sequence.

7. The process of claim 1 wherein said message comprises a side-channel.

8. A process for transmission of messages in a system, said process comprising the steps of sending, receiving, or propagating 1) more than one packet and 2) an interpacket gap, said packet comprising a start-of-stream delimiter, and a series of at least 16 information bytes encoded in symbols uninterrupted by a control symbol wherein said packet includes a plurality of non-standard symbols as part of a message.

9. The process of claim 8 wherein said interpacket gap includes both at least one symbol decoded as an Idle symbol and at least one non-Idle symbol such that the presence of said non-Idle symbol is part of a message.

10. The process of claim 9 wherein said system compromises Fast Ethernet.

11. The process of claim 10 wherein said non-Idle symbol is the symbol for zero.

12. The process of claim 10 wherein said non-Idle symbol is a symbol having only one zero bit.

13. The process of claim 9 wh rein said system comprises Gigabit Ethernet.

14. The process of claim 13 wherein said non-Idle symbol comprises a K28.5/Dxx.y or K28.1/Dxx.y sequence.

15. A transmitter for a signal, said signal comprising a plurality of packets and an interpacket gap, and wherein said transmitter includes 1) a buffer for a message to be inserted into said interpacket gap, 2) a formatter that modifies the bit stream representing said message to allow identification of message boundaries and to allow establishment of word alignment within said bit stream, and 3) an encoder that substitutes at least one symbol into said interpacket gap for at least one of said symbols decoded as an Idle symbol to encode at least a portion of said message into said interpacket gap.

16. The transmitter of claim 15 wherein said formatter modifies said bit stream with ah HDLC flag.

17. The transmitter of claim 16 wherein a logic zero is inserted by said formatter to avoid recognition of a portion of said message as said flag.

18. The transmitter of claim 15 wherein said signal comprises an Ethernet signal.

19. The transmitter of claim 15 wherein said substitution by said encoder represents a logic 1.

20. The transmitter of claim 15 wherein said substitution by said encoder represents a logic 0.